MINIATURIZED LOW NOISE VARIABLE MMIC AMPLIFIERS WITH LOW POWER CONSUMPTION FOR L-BAND PORTABLE COMMUNICATION APPLICATIONS

Shinji Hara, Kohsuke Osato, Atsushi Yamada, Toshiya Tsukao,
and Toshihiko Yoshimasu
Sharp Corporation Research and Development Group
2613-1 Ichinomoto-cho, Tenri, Nara 632, Japan
Phone +81-7436-5-1321

ABSTRACT

Miniaturized L-band low noise variable gain amplifiers are demonstrated for portable mobile communication equipment applications. The fabricated MMICs use D-mode GaAs MESFETs and need only positive bias. The amplifier has a noise figure of 3 dB and a gain of 14 dB. The chip size is approximately 1 mm x 1 mm and the current dissipation is only 1.8 mA.

INTRODUCTION

MMICs are very attractive for use in portable mobile communication equipment [1]. In such applications, the requirements for the front-end low noise amplifier include low current consumption, small size, and a high third order intercept point. Also, positive bias operation is preferable for battery operation of portable equipment.

This paper reports low noise variable gain amplifiers that operate without a negative bias. Furthermore, these amplifiers have low current consumption by using D-mode FETs instead of the conventional E-mode FETs [2,3].

CIRCUIT DESIGN

The noise figure of a microwave low noise amplifier is determined by the noise characteristics of the FET and input matching circuit. The minimum noise figure of the FET NFmin increases linearly as the frequency increases [4]. On the other hand, the loss of the input matching network is, roughly speaking, inversely proportional to frequency. Therefore, the dominant factor determining the noise figure of the circuit is the loss of the input matching circuit at lower frequencies, such as L-band, where the minimum noise figure of the FET is not so important, as shown in figure 1.

There are two methods to reduce the loss of the input matching circuit. One is to reduce the line loss itself by using wider and thicker metal, but it results in a larger chip size. The other method is to reduce the ratio of the impedance transformation of the network in order to shorten the line length. For that method, lower equivalent noise resistance Rn and lower optimum reflection coefficient $|\Gamma opt|$ are more important than a lower minimum noise figure for L-band low noise amplifier design [2].

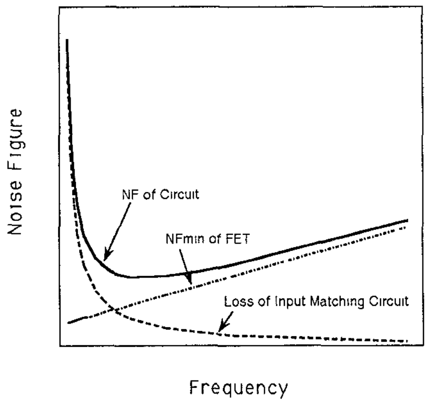

Fig.1 Generalized frequency characteristics of the circuit noise figure.

Noise parameters $|\Gamma opt|$, Rn, and NFmin versus the gate width of the FET and the current are plotted in figure 2 and 3, respectively. The FET is an ion implanted FET with 0.6 μm gate length. A commercially available on-wafer noise parameter test set was used for characterizing the FETs. Figure 2 shows that the

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wider gate width FET has lower $|\Gamma opt|$ and Rn. Figure 3 shows that very low current operation results in higher $|\Gamma opt|$, Rn, and NFmin. Also very low current operation results in a much lower available gain and linearity. Therefore, the choice of the optimum gate width is very important to realize a low noise amplifier in the low current condition. We chose 0.6 μm gate length and 300 μm gate width FETs.

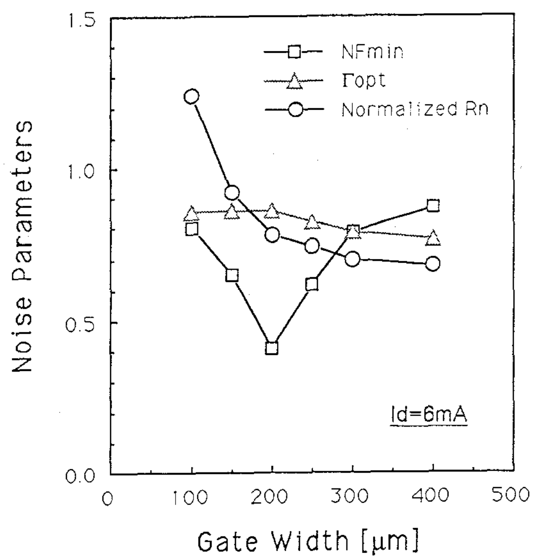

Fig.2 Noise parameters versus FET gate width. (Vds=1.5V)

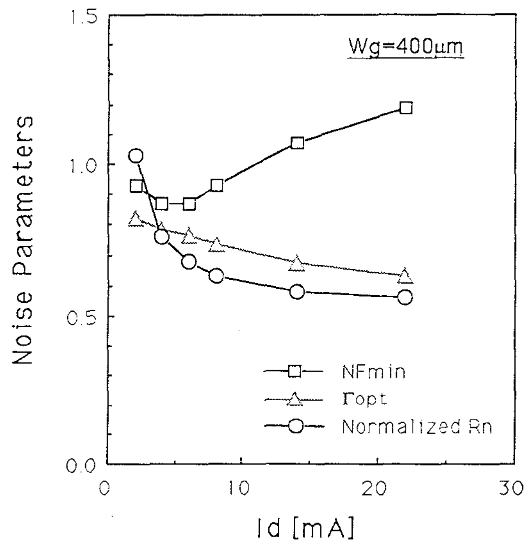

Fig.3 Noise parameters versus bias current. (Vds=1.5V)

Figure 4 shows the circuit schematic of the fabricated low noise amplifier. A cascode connected FET is used for higher gain and gain controllability. A conventional self-bias technique is used for positive bias operation. The circuit employs spiral inductors having 10 μm line width and 5 μm spacing to realize the small chip size. To reduce the loss of the spiral inductor and still use the conventional fabrication techniques, we used a stacked spiral inductor in which a contact hole connects the lower metal and upper metal. In the spiral inductor model, the equivalent circuit parameters are described as a function of the total line length [5]. Figure 5 shows a photograph of the fabricated 1.6 GHz low noise amplifier chip. The chip size is 0.94 mm x 1.15 mm.

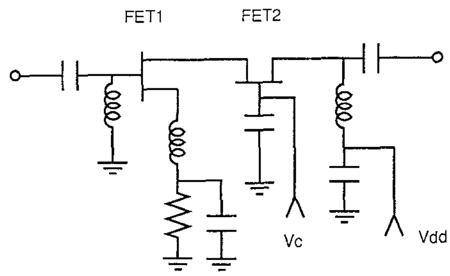

Fig.4 Circuit schematic of the fabricated low noise amplifier.

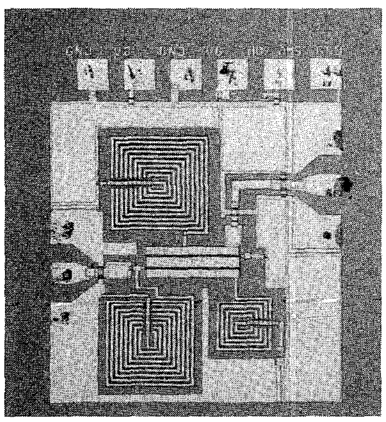

Fig.5 Photograph of the chip.

PERFORMANCE

Figure 6 shows typical frequency dependencies of the noise figure and gain for the 1.6 GHz low noise amplifier. The amplifier had a current dissipation of 1.8 mA and a bias voltage of 3 V. The gain control voltage Vc was 1.4 V. The minimum noise figure was 3.0 dB with a gain of 14 dB. The third order intercept point IP3 of 6.5 dBm was obtained.

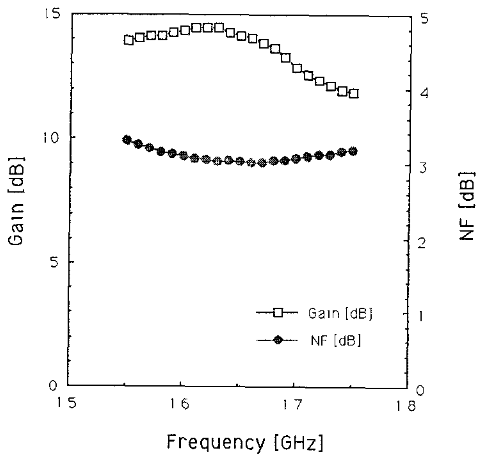

Fig.6 Frequency characteristics of the amplifier.

Figure 7 shows the gain control characteristics of the amplifier. Conventionally, a negative control voltage is used in this type of amplifier, but the noise figure degrades with the decrease in gain, and negative voltage is not preferable for battery operated equipment. For these reasons, we used positive voltage for the control voltage, so that the gain drops as the second gate voltage is increased toward the drain voltage[7]. The conventional amplifier can be simulated as a 2 stage amplifier in which the first amplifier is used for the gain control, whereas this one can be simulated as a 2 stage amplifier in which the second amplifier is used for gain control. In this design, the parameters of FET1 are almost constant at every control bias point. Therefore, the input matching condition and the noise figure do not change much even at the lower gain condition. The gain can be controlled from 15 dB to 3 dB with only a 0.6 dB NF degradation. The low power dissipation performance was measured by reducing the bias voltage Vdd, where Vc was almost half of Vdd. Figure 8 shows the measurement results. A maximum gain/power quotient [2] of 4.2 dB/mW was obtained. A 2 GHz amplifier with the same circuit configuration was also fabricated. The amplifier, which has a 0.9 mm x 1.1 mm chip size, can be controlled from 14 dB to -3 dB gain with a 2 dB NF degradation.

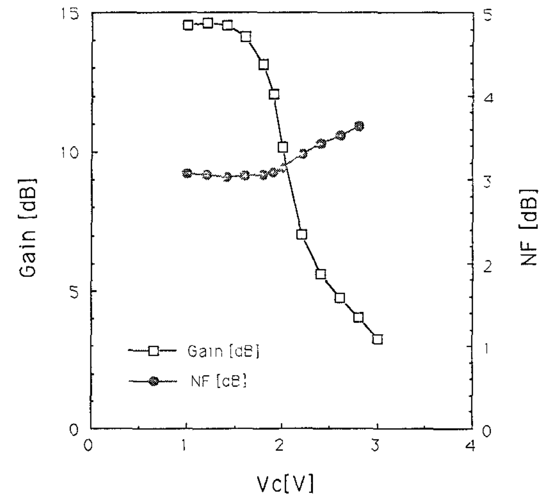

Fig.7 Gain control characteristics of the amplifier.

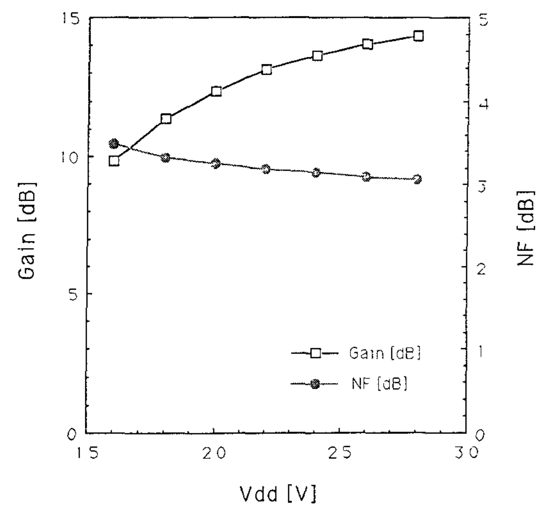

Fig.8 DC bias versus gain and noise figure.

Figure 9 compares our results with previous work. Gain/(NF*P_{DC}), which is an adequate figure of merit for low noise amplifiers for portable communication equipment, is plotted on the x axis. The chip size is plotted on the y axis. In figure 9, only self-biased MMICs appear. This circuit configuration using the cascode FET is suitable for the low noise amplifier with low current consumption. Also, it is more suitable for the MAMAS (Microwave Analogue MAster Slice) technique, better than a dual gate FET configuration. We have developed a low noise amplifier for the Japanese digital cellular (JDC) and cordless Personal Handy Phone (PHP) by using this configuration with plated spiral inductors. The JDC has 17 dB gain and a 2.5 dB noise figure and the PHP has 14 dB gain and a 2.7 dB noise figure [8].

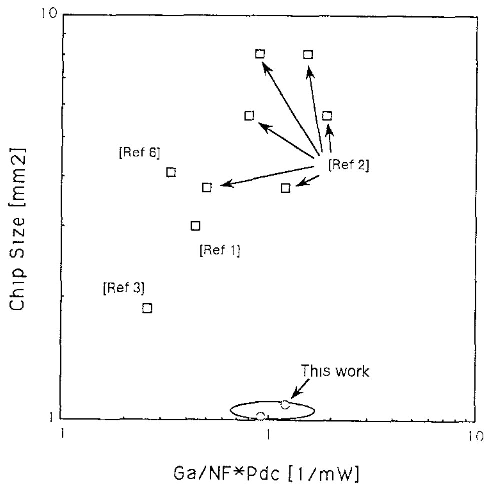

Fig.9 Comparison of this work with previous work.

CONCLUSION

Variable gain MMIC amplifiers were demonstrated for L-band portable mobile communication equipment. The amplifiers have the following features:

1. Very low power dissipation
2. Small size
3. Positive bias operation
4. Suitable configuration for MAMAS
5. Low noise characteristics

References

[1] Y. Imai et al., "Design and performance for low-current GaAs MMICs for L-band front-end applications, " *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-39, pp. 209-215, Feb. 1991.

[2] K. R. Cioffi, "MONOLITHIC L-BAND AMPLIFIERS OPERATING AT MILLIWATT AND SUB-MILLIWATT DC POWER CONSUMPTIONS," *IEEE 1992 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest*, pp. 9-12, June 1992.

[3] V. Nair, "Low Current enhancement mode MMICs for portable communication applications," *IEEE GaAs MMIC Symp. Tech. Dig.*, pp. 67-69, Oct. 1989.

[4] H. Fukui, "Design of Microwave GaAs MESFET's for Broad-Band Low-Noise Amplifiers," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-27, pp. 643-650, July 1979.

[5] M. Furukawa et al., "The Equivalent Circuit Modeling of Spiral Inductors including the Skin Effect", *Proc. 1993 IEICE Spring Conference*, C-115, March 1993. (in Japanese)

[6] K. Ohtsuka et al., "1.9-GHz-BAND LOW NOISE MMIC AMPLIFIER WITH LOW POWER CONSUMPTION," *National Convention Records of IEICE*, C-71, March 1992. (in Japanese)

[7] C. A. Liechti, "Performance of Dual-Gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," *IEEE Trans. on Microwave Theory and Techniques*, vol. MTT-23, pp. 461-46, June 1975.

[8] K. Osato et al., "LOW NOISE MMIC AMPLIFIERS FOR DIGITAL MOBILE COMMUNICATION APPLICATION," *National Convention Records of IEICE*, C-77, March 1993. (in Japanese)